MimicPro™ FPGA PROTOTYPING SYSTEM

For Fastest ASIC Prototyping and Debugging

The Corigine© MimicPro Prototyping System is a high-performance, FPGA-based system that raises prototyping to an unprecedented new level. The MimicPro system enables early software development, system validation and regression testing, while significantly reducing development time and workload.

Corigine MimicPro Prototyping System (32-FPGA)

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The Corigine MimicPro Prototyping System provides performance and speed for ASIC and software development for both enterprise and cloud operation, with utmost security and scalability.

FASTER DEVELOPMENT

The Corigine MimicPro system is the industry's next-generation platform for automating prototyping including manual partitioning operations, while providing a system-level view for optimum partitioning and performance. In addition, the MimicPro system adds deep local debug capabilities providing much greater visibility and faster elimination of bugs. Thus the MimicPro system reduces the overall development time and cost-effectively accelerates software development without the dependence on costly emulation.

SCALABILITY

The Corigine MimicPro system provides modular upgrabiliy for the enterprise's ASICs family of AI, Processor, Vision, Communication and other SOCs. The MimicPro solution provides scalability from 1 to 32 FPGAs. The system also provides easy upgrability to the latest available FPGAs.

CLOUD ACCESS & SECURITY

The Corigine MimicPro system has been architected for opration in both the Enterprise and Cloud environments. Also, the design enables security of the user IP thru encrypted prototyping.

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Corigine MimicPro Prototyping System Key Features and Benefits:

Features	Benefits
User Design Import	Support Verilog, System Verilog, VHDL and gate level Edif
RTL grouping for synthesis	Reduces large design operations and manual errors
Automatic clock handling	Eliminate the needed for manual handling of gated clock thus reducing workload and human errors
Auto-Partition	Reduce R&D workload
System level routing	Best system performance for software development
Local debug, system scope	High visibility for faster logic debug, Greater visibility by orders of magnitude
Probe ECO	Minimize compilation time
Memory compiler/memory analyzer	For backdoor pick and poke for user memory eliminating time consuming recompile
Monitor all the F/F	Snapshot all the user design state machine
Fault injection/Force Release	Support automotive safety requirement
User AXI master port	Transfer the data using AXI IP and port
Multiple user, cloud friendly	Multiple user to support cloud application or internal FPGA farm
Speed bridge supported	PCIe, Ethernet, Sata, USB, DDR, HDMI…etc

Specifications:

- Scalable: 30 million to 1 billion gates (1 to 32 FPGAs)
- Built-in Memory analyzer, Memory compiler
- Parallel synthesis, parallel place and route
- Timing driven auto-partitioning
- Automated gated-clock conversion
- System scope with local memory for debug
- Fault injection, Force/Release for safety
- Runtime control for clock generation circuit
- Vector mode enabling cloud deployment and regression testing
- Built-in monitor and readback for all design flip-flops
- FMC interface boards: HDMI, USB, SD,UART, JTAG, SPI-Flash, DDR4

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